

METHOD AND SYSTEM FOR PROVIDING INTERACTIVE TESTING OF INTEGRATED CIRCUITS

A method for providing interactive and iterative testing of integrated circuits including the receiving of a first failing region. The first failing region corresponds to one or more circuits on the integrated circuit. The method generates a set of adaptive algorithmic test patterns for the one or more circuits in response to the first failing region and to a logic model of the integrated circuit. Expected results for the test patterns are determined. The method includes applying the test patterns to the first failing region on the integrated circuit resulting in actual results for the test patterns. The expected results to the actual results are compared. The method also transmits mismatches between the expected results and the actual results to a fault simulator. The method includes receiving a second failing region from the fault simulator, the second failing region created in response to the mismatches and the logic model, and the second failing region corresponding to a subset of the one or more circuits on the integrated circuit.